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Set Items Description
S1 77832 S (COMPRESS? OR ZIP? ? OR ZIPPED OR ZIPPING OR STUFF??? OR WINZIP? OR SQUEEZ? OR COMPACT???)(5N)(DATA OR DATUM OR FILE? ? OR INFORMATION OR CONTENT? ? OR RECORD? ? OR DATABASE? OR DATA()BASE? OR REPOSITOR? OR RESOURCE? ?)
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S5 5 S S2(5N)(CARE(2W)(BIT? ? OR BYTE? ? OR CODE? ?))
S6 5 S S5(10N)S4
S7 0 S S3(15N)S6
S8 254262 S S4(10N)((LESS OR SMALLER OR LOWER OR LOOSEN OR BELOW OR FEWER OR MINOR?)(3N)(NUMBER? ? OR NUMERAL? ? OR CHARACTER? ? OR VALUE? ? OR DATA OR INFORMATION OR FIGURE? ? OR DIGIT? ? OR INTEGER? ? OR BIT? ? OR BYTE? ? OR WORD? ? OR CONTENT? ? OR AMOUNT? ? OR QUANTIT??? OR PATTERN? ? OR SEQUENCE? ? OR SERIES? ? OR STREAM? ?))
S9 28 S S2 AND (CARE(2W)(BIT? ? OR BYTE? ? OR CODE? ?))
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S11 3 S S10 AND S9

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Subject summary

? t /3,k/all
11/3,K/1 (Item 1 from file: 350) Links
Fulltext available through: Order File History
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0009546905 & & *Drawing available*
WPI Acc no: 1999-492406/199941
XRPX Acc No: N1999-378102
Pattern generator for VLSI chip testing
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
RD 424078	A	19990810	RD 1999424078	A	19990720	199941	B

Priority Applications (no., kind, date): RD 1999424078 A 19990720

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
RD 424078	A	EN	3	2	

Pattern generator for VLSI chip testing Alerting Abstract ...NOVELTY - Pattern generator stores a seed of the final test pattern with less bits than the test pattern but more bits than the number of final care bits. The generator then expands the seed by reproducing the correct patterns of the care bits and filling the other bit position with random values. Seeds are part of the stored pseudo technology independent test evaluation system (TITES) code. The... ...equations to produce a solution of the form CCCC...CCC1000...000, C being a code bit. The end of the code is redundant and can be omitted, the resulting code CCCC... ...DESCRIPTION OF DRAWINGS - The drawing shows expansion of the seed to fill the full test pattern. Title Terms /Index Terms/Additional Words: PATTERN; Class Codes

11/3,K/2 (Item 2 from file: 350) Links
Fulltext available through: Order File History
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0009546903 & & *Drawing available*
WPI Acc no: 1999-492404/199941
XRPX Acc No: N1999-366676
Pattern generator for VLSI chip testing
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Patent Family (1 patents, 1 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
RD 424076	A	19990810	RD 1999424076	A	19990720	199941	B

Priority Applications (no., kind, date): RD 1999424076 A 19990720

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes
RD 424076	A	EN	4	3	

Pattern generator for VLSI chip testing Alerting Abstract ...NOVELTY - Pattern generator stores a seed of the final test pattern with less bits than the test pattern but more bits than the number of final care bits. The generator then expands the seed by reproducing the correct patterns of the care bits and filling the other bit position with random values. Seeds are part of the stored pseudo technology independent test evaluation system (TITES) code. The generator has linear feedback shift registers with prime or Mersenne number cycle lengths. The pattern is generated by the seed being loaded via the scan paths of the shift registers, clock pulses being applied to the pattern generator so that another bit of the test pattern appears at the output of the cascade with each clock pulse ... ...USE - Pattern generator is for testing VLSI chips... ...DESCRIPTION OF DRAWING(S) - The drawing shows expansion of the seed to the full test pattern. Title Terms /Index Terms/Additional Words: PATTERN; Class Codes

11/3,K/3 (Item 3 from file: 350) Links
Fulltext available through: Order File History
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0007387076 & & *Drawing available*
WPI Acc no: 1995-322700/199542
Related WPI Acc No: 1994-009121; 1995-346813; 1995-360866; 1996-173495; 1999-073217; 1999-073219; 1999-073218; 1999-083979; 1999-073222; 1999-073221; 1999-073220; 1998-365305; 1996-079507; 1995-346814; 1995-322737
XRPX Acc No: N1995-242923

RAM accessing method of number of words that is less than predetermined fixed burst length - including enable line to selectively enable and disable reading and writing to RAM by ordering N words which are read from or written to RAM and disabling RAM upon determining M words which are read from or written to RAM
Patent Assignee: BOYD K J (BOYD-I); CLAYDON A P J (CLAY-I); DISCOVISION ASSOC (MCAC); FINCH H R (FINC-I); JONES A M (JONE-I); ROBBINS W P (ROBB-I); SOTHERAN M W (SOTH-I); WISE A P (WISE-I)
Inventor: ADRIAN P W; ANTHONY M J; BARNES D A; BARNES M; BIRCH N; BOYD K J; CLAYDON A P J; DEWAR K D; DONALD W W P; FINCH H R; HELEN R F; JONES A M; KULIGOWSKI A P; MARTIN W S; PATERSON D W W; PATTERSON D W W; ROBBINS W P; SMITH C; SOTHERAN M; SOTHERAN M W; WILLIAM P R; WISE A P
Patent Family (77 patents, 17 & countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
GB 2287808	A	19950927	GB 19953964	A	19950228	199542	B
EP 674266	A2	19950927	EP 1995301272	A	19950228	199543	E
EP 674442	A2	19950927	EP 1995301299	A	19950310	199543	E
EP 674443	A2	19950927	EP 1995301301	A	19950228	199543	E
EP 674446	A2	19950927	EP 1995301300	A	19950228	199543	E
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			US 1995400397	A	19950307		
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GB 2288521	B	19981014	GB 19954047	A	19950228	199843	E
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CA 2145361	C	19990907	CA 2145361	A	19950323	200003	E
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			US 1995399801	A	19950307		
			US 1995400397	A	19950307		
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JP 2001128108	A	20010511	JP 1995202691	A	19950324	200133	E
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DE 69520893	E	20010613	DE 69520893	A	19950228	200141	E
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			US 1999323627	A	19990601		
US 20040019775	A1	20040129	US 199382291	A	19930624	200416	E
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			JP 1995202691	A	19950718		

Priority Applications (no., kind, date): EP 1992306038 A 19920630; GB 19945914 A 19940324; GB 199415365 A 19940729; GB 199415387 A 19940729; GB 199415391 A 19940729; GB 199415413 A 19940729; GB 19953964 A 19950228; GB 19954019 A 19950228; US 1995400211 A 19950307; US 1995479279 A 19950607; US 1995487224 A 19950607

Patent Details

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GB 2287808	A	EN	75	25		
EP 674266	A2	EN	40			
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EP 674442	A2	EN	552	169		
Regional Designated States,Original	AT BE CH DE FR GB IE IT LI NL					
EP 674443	A2	EN	502	169		
Regional Designated States,Original	AT BE CH DE FR GB IE IT LI NL					
EP 674446	A2	EN	494	169		

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CA 2145379	A	EN				
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US 5625571	A	EN	12	7		
US 5689313	A	EN	10	3	Division of application	US 1995399801
US 5699544	A	EN	10	9	Continuation of application	US 199382291
					C-I-P of application	US 1995382958
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					Division of application	US 1995400397
US 5724537	A	EN	202	81	Division of application	US 1995399799
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					Division of patent	EP 674443
Regional Designated States,Original	AT BE CH DE FR GB IE IT LI NL					
EP 891088	B1	EN			Division of application	EP 1995301301
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JP 2001128108	A	JA	25		Division of application	JP 1995202691
DE 69520852	E	DE			Application	EP 1995301301
					Based on OPI patent	EP 674443
DE 69520893	E	DE			Application	EP 1998202132
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DE 69520894	E	DE			Application	EP 1998202133
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EP 674446	B1	EN				
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DE 69521927	E	DE			Application	EP 1995301300
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US 6297857	B1	EN			Division of application	US 1995474231
KR 275427	B	KO			Previously issued patent	KR 95033862
US 6330666	B1	EN			Continuation of application	US 199382291
					C-I-P of application	US 1995382958
					Continuation of application	US 1995400397
US 6378030	B1	EN			Continuation of application	US 1995399799
					Continuation of application	US 1997810780
					Division of application	US 1997950892
					Division of patent	US 5956741
US 6417859	B1	EN			Continuation of application	US 1995399801
					Division of application	US 1997876720
					Division of patent	US 6034674
US 20040019775	A1	EN			Continuation of application	US 199382291
					C-I-P of application	US 1995382958
					Continuation of application	US 1995400397
					Division of application	US 1997307239
					Division of patent	US 6330666
US 20040025000	A1	EN			Continuation of application	US 199382291
					C-I-P of application	US 1995382958
					Continuation of application	US 1995400397
					Division of application	US 1997307239
					Division of patent	US 6330666
EP 1026600	B1	EN			Division of application	EP 1995301272
					Division of patent	EP 674266
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DE 69533630	E	DE			Application	EP 2000201754
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Original Publication Data by AuthorityArgentinaPublication No. ...Original Abstracts:address generator, clearing the buffers for occupation by subsequently arriving data, and maintaining status information concerning the buffers. The buffer manager also examines tokens of received data in order to update the status of the arrival buffer. ... ... This invention provides a method to control the buffering of encoded video data organized as frames or fields. This method involves determining the picture number of each incoming decoded... ... This invention discloses a method for accessing Dynamic Random Access Memory (DRAM)to store and retrieve data words associated with a two dimensional image. The DRAM includes two separate banks, a first bank and a second bank. Each bank is capable of operating in page mode to read and write the data words. The two dimensional image is organized in a two dimensional grid pattern of cells, each cell containing an M by N matrix of pixels. The words associated with... ... Each cell is assigned a particular one of the two banks so that all data words associated with that particular cell are read from and written to one particular page of that particular bank. The assignment of banks to cells is done such... ... in the same row or in the same column. There is then read the data
words associated with a cell that is composed of a matrix of pixels and is not aligned with the two dimensional grid pattern, but is aligned with pixels in cells in the two dimensional grid pattern. ... ... A pipeline video decoder and decompression system handles a plurality of separately encoded bit streams arranged as a single serial bit stream of digital bits and having separately encoded pairs of control codes and corresponding data carried in the serial bit stream. The pipeline system employs a plurality of interconnected stages to decode and decompress the single bit stream, including a start code detector. When in a search mode, the start code detector searches for a specific start code corresponding... ... one of multiple compression standards. The start code detector responding to the single serial bit stream generates control tokens and data tokens. A respective one of the tokens includes a plurality of data words. Each data word has an extension bit which indicates a presence of additional words therein. The data words are thereby unlimited in number. A token decode circuit positioned in certain of the stages recognizes certain of the tokens as control tokens pertinent to that stage and passes unrecognized control tokens to a succeeding stage. A reconfigurable decode and parser processing means handle an identified data token. Methods relating to the decoder and decompression system include processing steps relating thereto. A configurable RAM interface connecting a bus to RAM is adapted to receiving large multiword variable length tokens at a high data arrival rate, using a swing buffer and a buffer manager. An address source provides complete addresses to the interface. The buffer manager has a state machine which transitions among a plurality of states, maintaining status information about the buffers, allocating the buffers for reference by a write address generator, clearing the buffers for occupation by subsequently arriving data, and maintaining status information concerning the buffers. The buffer manager also examines tokens of received data in order to update the status of the arrival buffer... ...This invention provides a method to control the buffering of encoded video data organized as frames or fields. This method involves determining the picture number of each incoming decoded ...Claims:access system comprising:a RAM responsive to low level commands;a state machine generating a string of low level commands in response to a received high level command, the state machine having modes, wherein the string of low level commands generated in response to the high level command received in one mode differs from the string of low level commands generated in response to the high level command received in another mode... ... A method of accessing from RAM a number M of words that is less than the predetermined fixed burst length N of the RAM, the RAM including an enable line that selectably enables and disables reading from and writing to the RAM, the method consisting in:ordering N words to be read from... ... determining when M words have been read from or written to the RAM, M being less than N; anddisabling the RAM upon determining M words had been read from or written... ... 1. A method of accessing from RAM a number M of words that is less than the predetermined fixed burst length N of the RAM, the RAM including an enable... ... method characterized by:
ordering N words to be read from or written to the RAM;
determining when- M words have been read from or written to the RAM, M being less than N; and... ... 1. In a system having an input, an output and a plurality of processing stages between the input and the output, the improvement characterized by:
said plurality of processing stages are interconnected by a two-wire interface for conveyance of tokens along said pipeline; and control and/or DATA tokens in the form of universal adaptation units for interfacing with all of said stages in said pipeline and interacting with selected stages in said pipeline,
whereby said processing stages in said pipe-line are afforded enhanced flexibility in configuration and processing..... A system having an input, an output and a plurality of processing stages between the input and the output,said plurality of processing stages being interconnected into a pipeline by a two-wire interface for conveyance of control and/or DATA tokens along said pipeline, one wire for each of a VALID transfer control signal and an ACCEPT transfer control signal respectively;each of said control and/or DATA tokens being a universal adaptation unit in the form of an interactive interfacing messenger package for control and/or data functions, for interfacing with all of said stages in said pipeline and for interacting with selected stages in said pipeline, said system being characterised by:a reconfigurable processing stage (48) comprising a token decode circuit (33) for receiving tokens, an action identification unit (39) responsive to a recognised control token, and a processing unit (36) for processing data under the control of said action identification circuit (39),said reconfigurable processing stage (48) being reconfigurable in response to recognition of a selected token, and said token decode circuit (33) providing a proper flag or index signal (37) to said processing unit (36) to alert said processing unit (36) to the presence... ..... entree, une sortie et plusieurs etages de traitement situes entre l'entree et la sortie,lesdits plusieurs etages de traitement etant relies les uns aux autres de maniere a former un... ... des jetons de DONNEES le long dudit pipeline, les fils etant chacun destines a un signal de controle de transfert VALID ("VALIDE") et a un signal de controle de transfert ACCEPT ("ACCEPTER"), respectivement;chacun desdits jetons de controle et/ou jetons... ... de traitement reconfigurable (48) comportant un circuit de decodage de jetons (33) destine a recevoir les jetons, une unite d'identification d'action (39) sensible a un jeton de controle reconnu, et une unite de traitement (36) destinee a traiter les... ... reconnaissance d'un jeton selectionne, et ledit circuit de decodage de jetons (33) envoyant un signal d'indicateur ou d'index (37) approprie a ladite unite de traitement (36) pour alerter... ... 1. In a system having an input and an output and a plurality of processing stages between the input and the output, the improvement

characterized by:
an interactive interfacing token, defining a universal adaptation unit for control and/or data functions among said processing stages; and
one of said stages receiving said input and adapted to generate and/or convert said tokens... ... System zur Handhabung einer Vielzahl von getrennt kodierten Bitstromen, die in Form eines seriellen Bitstroms aus digitalen Bits angeordnet sind und getrennt kodierte Paare von Startkodes aufweisen und Daten, die in dem seriellen Bitstrom gefuhrt sind,welches System einen Eingang, einen Ausgang und eine Vielzahl von verarbeitenden Stufen zwischen dem Eingang und dem Ausgang aufweist,wobei die Vielzahl der verarbeitenden Stufen durch ein Zweidraht-Interface zu einer Pipeline verbunden sind, um Steuer-und/oder DATEN-Token entlang... ... zu erzielen und um eine Wechselwirkung mit ausgewahlten Stufen in der Pipeline zu realisieren, undeine der Stufen die Eingangsgrosse empfangt und dafur ausgebildet ist, um die Token zu generieren und... ... umfasst, die in serieller Weise verbunden sind, wobei jedes der Register eine unterschiedliche Zahl von Bits aus dem seriellen Bitstrom speichert,der Startkodedetektor ferner einen Detektor (225) aufweist, um das Vorhandensein... ... A system for handling a plurality of separately encoded bit streams arranged as a serial bit stream of digital bits and having separately encoded pairs of start codes and data carried in the serial bit stream,said system having an input, an output and a plurality of processing stages between the input and the output,said plurality of processing stages being interconnected into a pipeline by a two-wire interface for conveyance of control and/or DATA tokens along said pipeline, one wire for each of a VALID transfer control signal and an ACCEPT transfer control signal respectively;each of said control and/or DATA tokens being a universal adaptation unit in the form of an interactive interfacing messanger package for control and/or data functions, for interfacing with all of said stages in said pipeline and for interacting with selected stages in said pipeline, andone of said stages receiving said input and being adapted to generate and/or convert said tokens, said system being characterised by:a Start Code Detector (SCD 51) for receiving input over said two-wire interface (52) and for generating one of said tokens;said Start Code Detector comprising a value register (221), a decode register (224) and a value decode shift register (230) connected in serial fashion, each of said registers storing a different number of bits from the serial bit stream,said Start Code Detector further comprising a detector (225) for detecting the presence or absence of a start code, a value decoder (228) for accepting data from said value decode shift register (230) in parallel, and an index-to-tokens converter (234) for converting information into one of said tokens.... ... Systeme pour traiter une pluralite de flux binaires codes separement se presentant sous la forme d'un flux binaire serie compose de bits numeriques et comportant des paires, codees separement, de codes de debut et de donnees transportees dans le flux binaire serie,ledit systeme comportant une entree, une sortie et plusieurs etages de traitement situes entre l'entree et la sortie,lesdits plusieurs etages de traitement etant relies les uns aux autres de maniere a former un pipeline via une interface a deux fils destinee a acheminer des jetons de controle et/ou des jetons de DONNEES le long dudit pipeline, un fil etant destine a un signal de controle de transfert VALID ("VALIDE") et un fil etant destine a un signal de controle de transfert ACCEPT ("ACCEPTER"), respectivement,lesdits jetons de controle et/ou jetons de... ... dudit pipeline et a interagir avec des etages selectionnes dudit pipeline, etun premier desdits etages recevant ladite entree et etant adapte pour generer et/ou convertir lesdits jetons, ledit systeme... ... de decodagede valeur (230) montes en serie, chacun desdits registres memorisant un nombre different de bits du flux binaire serie,ledit Detecteur de Codes de Debut comportant en outre un detecteur (225) pour detecter la presence ou l'absence d'un code de debut, un decodeur de valeur... 1. In a system having an input, an output and at least one processing stage between the input and the output, the improvement characterized by:
said processing stage is configurable in response to... ... one token in the form of a universal adaptation unit for establishing control and/or data functions,
whereby said processing stage is afforded enhanced flexibility in configuration and processing. ... ... universalen Anpassungseinheit in Form eines interaktiven koppelnden Nachrichten-oder Boten-Paketes fur Steuer-und/oder Daten-Funktionen ist, um eine Kopplung mit all den Stufen in der Pipeline zu bewirken, und um mit ausgewahlten Stufen in der Pipeline in Wechselwirkung zu treten... ... rekonfigurierbare verarbeitende Stufe (48), die im Ansprechen auf das Erkennen eines ausgewahlten Tokens rekonfigurierbar ist, wobei die Wechselwirkung des ausgewahlten Tokens mit der genannten verarbeitenden Stufen durch die fruhere Verarbeitungs-Geschichte... ... A system having an input, an output and a plurality of processing stages between the input and the output,said plurality of processing stages being interconnected into a pipeline by a two-wire interface for conveyance of control and/or DATA tokens along said pipeline, one wire for each of a VALID transfer control signal and an ACCEPT transfer control signal respectively;each of said control and/or DATA tokens being a universal adaptation unit in the form of an interactive interfacing messanger package for control and/or data functions, for interfacing with all of said stages in said pipeline and for interacting with... ... 33) for recognizing and decoding said selected token, and register means (43, 44) for holding information stored from previously decoded tokens;whereby reconfigurable processing is performed as configured by said action identification circuit (39) on the basis of the information stored in said register means (43, 44), of said selected token and of said history state.Systeme comportant une entree, une sortie et plusieurs etages de traitement situes entre l'entree et la sortie,lesdits plusieurs etages de traitement etant relies les uns aux... ... interface a deux fils destinee a acheminer des jetons de controle et/ou des jetons DATA ("DONNEES") le long dudit pipeline, un fil etant destine a un signal de controle de transfert VALID ("VALIDE") et un fil etant destine a un signal de controle de transfert ACCEPT ("ACCEPTER"), respectivement,lesdits jetons de controle et/ou jetons DATA etant chacun une unite d'adaptation universelle se presentant sous la forme d'un ensemble... etages dudit pipeline et a interagir avec des etages selectionnes dudit pipeline,ledit systeme etant caracterise par:un etage de traitement reconfigurable (48) pouvant etre reconfigure en reponse a la reconnaissance d'un jeton selectionne, l'interaction dudit jeton selectionne avec ledit etage de traitement etant conditionnee par l'historique des traitements precedents dudit etage de traitement... ... par ledit circuit d'identification d'action (39) sur la base des informations memorisees dans lesdits moyens de registres (43, 44), dudit jeton selectionne et dudit etat de l'historique.... ... inverse modeller stage and said inverse discrete cosine transform stage, responsive to tokens for processing data, wherein said tokens each comprise a plurality of data words, each said word including an extension indicator which indicates a presence or an absence... ... zur Handhabung einer Vielzahl von getrennt kodierten Bitstromen, die als ein serieller Bitstrom von digitalen Bits angeordnet sind,welches System einen Eingang, einen

Ausgang und eine Vielzahl von verarbeitenden Stufen zwischen... ... und/oder DATEN-Token entlang der Pipeline zu fordern, wobei ein Draht fur jedes der Signale gemass einem VALID-Transfer-Steuersignal und einem ACCEPT-Transfer-Steuersignal vorgesehen ist;jeder der Steuer... ... aufweist, der ein Vorhandensein oder ein Fehlen von zusatzlichen Worten in dem Token anzeigt; welches System gekennzeichnet ist durch:einen CODING... ... Register den CODING... ... der genannte CODING... ... A system for handling a plurality of separately encoded bit streams arranged as a serial bit stream of digital bits,said system having an input, an output and a plurality of processing stages between the input and the output,said plurality of processing stages being interconnected into a pipeline by a two-wire interface for conveyance of control and/or DATA tokens along said pipeline, one wire for each of a VALID transfer control signal and an ACCEPT transfer control signal respectively;each of said control and/or DATA tokens being a universal adaptation units in the form of an interactive interfacing messanger package for control and/or data functions, for interfacing with all of said stages in said pipeline and for interacting with selected stages in said pipeline, said tokens each including a plurality of data words, each of said words having an extension indicator which indicates a presence or an... ... cosine transform stage (83), said inverse quantizer stage (79) being responsive to tokens for processing data and remembering in a register said CODINGSTANDARD token as said CODINGSTANDARD token flows by said inverse quantizer stage (79), thereby remembering which one of said picture compression/decompression standards said inverse quantizer stage (79) is operating in.... ... binaires codes separement se presentant sous la forme d'un flux binaire serie compose de bits numeriques,ledit systeme comportant une entree, une sortie et plusieurs etages de traitement situes entre... ... interface a deux fils destinee a acheminer des jetons de controle et/ou des jetons DATA ("DONNEES") le long dudit pipeline, un fil etant destine a un signal de controle de transfert VALID ("VALIDE") et un fil etant destine a un signal de controle de transfert ACCEPT ("ACCEPTER"), respectivement,lesdits jetons de controle et/ou jetons DATA etant chacun une unite d'adaptation universelle se presentant sous la forme d'un ensemble de messagers d'interfacage interactifs destine a des fonctions de controle et/ou a... ... et rappeler dans un registre ledit jeton CODING... ... lorsque ledit jeton CODINGSTANDARD traverse ledit etage de quantification inverse (79), rappelant ainsi dans laquelle desdites normes de compression/decompression d'images ledit... ... 1. In a video decoding system having an input, an output and a plurality of pipelined sequential processing stages between the input and the output, comprising:
a plurality of two-wire interfaces interconnecting said stages for conveyance of variable length control and/or DATA tokens sequentially through said stages in the form of universal adaptation units for interfacing with... ... said receiver, said clock having transitions from
a first state to a second state, wherein data is transferred from said sender to said receiver upon a clock transition only when said... ... said conversion circuit;
a memory defining at least three buffers for storage of the encoded data, one of said buffers being a display buffer, and another of said buffers being an arrival buffer;
a write address generator for generating addresses for data being stored in said memory;
a read address generator for generating addresses for reading data stored in said memory; and
a buffer manager responsive to said arrival rate, said display... ... zur Handhabung einer Vielzahl von getrennt kodierten Bitstromen, die als ein serieller Bitstrom von digitalen Bits angeordnet sind,welches System einen Eingang, einen Ausgang und eine Vielzahl von verarbeitenden Stufen zwischen... ... Ausgang aufweist,die Vielzahl der verarbeitenden Stufen zu einer Pipeline mittels eines Zweidraht-Interfaces miteinander verbunden sind, um Steuer-und/oder DATEN-Token entlang der Pipeline zu fordern, wobei ein Draht jeweils fur ein VALID-Transfer-Steuersignal und ein ACCEPT-Transfer-Steuersignal dient, das Zweidraht-Interface einen Sender, einen Empfanger und ein mit dem Sender und dem Empfanger verbundenes Taktsignal aufweist, wobei das Taktsignal Ubergange von einem ersten... ... jeder der Steuer- und/oder DATEN-Token eine universelle Anpassungseinheit in Form eines interaktiven koppelnden Nachrichten- oder Boten-Paketes fur Steuer- und/oder Daten-Funktionen ist, um eine Kopplung mit all... ... an die Farbraum-Umsetzerschaltung angeschlossen ist,einen Speicher, der wenigstens drei Pufferstufen fur die Speicherung von Videodaten festlegt,einen Schreibadressengenerator zum Erzeugen von Adressen fur die Videodaten, die in dem Speicher gespeichert sind,einen Leseadressengenerator zum Erzeugen von Adressen fur Lese-Videodaten, die in dem Speicher gespeichert sind,und einen Puffermanager zum Empfangen der hereinkommenden Videoinformationen und um den Adressengeneratoren die Informationen uber die Zeitlage der Ankunft der Videoinformationen zuzufuhren und zwar in der Halbbildrate (frame... ... A system for handling a plurality of separately encoded bit streams arranged as a serial bit stream of digital bits,said system having an input, an output and a plurality of processing stages between the input and the output,said plurality of processing stages being interconnected into a pipeline by a two-wire interface for conveyance of control and/or DATA tokens along said pipeline, one wire for each of a VALID transfer control
signal and an ACCEPT transfer control signal respectively, said two-wire interface comprising a sender, a receiver, a clock connected to said... ... said receiver, said clock having transitions from a first state to a second state, wherein data is transferred from said sender to said receiver upon a clock transition only when said sender is ready and said receiver is ready;each of said control and/or DATA tokens being a universal adaptation unit in the form of an interactive interfacing messenger package for control and/or data functions, for interfacing with all of said stages in said pipeline and for interacting with... ... color space conversion circuit,a memory defining at least three buffers for storage of video data,a write address generator for generating addresses for video data being stored in said memory,a read address generator for generating addresses for reading video data stored in said memory,and a buffer manager for receiving incoming video information and supplying the address generators with information on the timing of arrival of said video information, on the frame rate of said video information, and on a selected display rate of said video information, whereby upon receiving a selected token said buffer manager determines the status of each buffer and the readiness of each of said buffers to accept new video data.... ... binaires codes separement se presentant sous la forme d'un flux binaire serie compose de bits numeriques,ledit systeme comportant une entree, une sortie et plusieurs etages de traitement situes entre l'entree et la sortie,lesdits plusieurs etages de traitement etant relies les uns aux autres de maniere a former un pipeline via une interface a deux fils destinee a acheminer des jetons de controle et/ou des jetons DATA ("DONNEES") le long dudit pipeline, un fil etant destine a un signal de controle de transfert VALID ("VALIDE") et un fil etant destine a un signal de controle de transfert ACCEPT ("ACCEPTER"), respectivement, ladite interface bifilaire comportant un emetteur, un recepteur, une horloge reliee audit emetteur et audit recepteur, ladite horloge ayant des transitions d'un premier etat

vers un second etat, dans lequel des donnees sont transferees a partir dudit... ... vers ledit recepteur lors d'une transition d'horloge uniquement lorsque ledit emetteur est pret et ledit recepteur est pret,lesdits jetons de controle et/ou jetons DATA etant chacun une unite d'adaptation universelle se presentant sous la forme d'un ensemble de messagers d'interfacage interactifs destine a des... ... ledit etage de formatage video comportant:un circuit de conversion de l'espace des couleurs,une memoire definissant au moins trois tampons pour la memorisation de donnees video,un generateur d'adresses d'ecriture pour generer des adresses pour des donnees video memorisees dans ladite memoire,un generateur d'adresses de lecture pour generer des adresses pour lire des donnees video memorisees dans ladite memoire,et un gestionnaire de tampons pour recevoir des informations video entrantes et fournir aux generateurs d'adresses des informations sur le cadencement de l'arrivee desdites informations video, sur la frequence-images desdites informations video, et sur une frequence d'affichage selectionnee desdites informations video, de sorte que, apres la reception d'un jeton selectionne, ledit gestionnaire de tampons determine l'etat de chaque tampon et la disponibilite de chacun desdits tampons a... ... 1. A pipeline processing machine having a plurality of reconfigurable processing stages interconnected by a two-wire interface bus, one of said processing stages being a... ... decoder; a second of said stages being a token generator for generating control tokens and data tokens for passage along said two-wire interface; said machine comprising:

a token decode means positioned in said spatial decoder for recognizing certain of said tokens as control tokens pertinent to said spatial decoder and for configuring said spatial decoder for spatially decoding said data tokens following said control token into a first decoded format; and

a further one of said stages being a temporal decoder positioned downstream... ... pertinent to said temporal decoder and for configuring said temporal decoder for temporally decoding said data tokens following said control token into a second decoded format. ... ... composed of partial words;

rotating a partial word to be accessed to a least significant bit justification;

extending a remaining part of a word which contains the partial word so that... ... the partial word with a termination marker, said substitution field being variable in size;

substituting data in all of said substitution field to define a part of an address of a ... 1. An apparatus for connecting a bus to a RAM comprising:

a single address generator providing complete addresses that is clocked at a first clock rate;

a RAM interface, comprising:

a plurality of swing buffers connected to a bus for receiving therefrom a plurality of data words from a source at a second clock rate;

a control coupled to said... ... wherein said two-wire link comprises a sender, a receiver, and a clock connected to said sender and said receiver, wherein data is transferred from said sender to said receiver upon a transition of said clock... ... wherein the interface is clocked at a third clock rate that is asynchronous with said first clock rate and said second clock rate, and data is transferred between a selected swing buffer and a RAM in response to a first signal that is generated by said control when said control receives an address from the address generator and said control receives a second signal from said selected swing buffer via said communication link. ... ... for connecting a bus to RAM comprising:

a bus configuration register for specifying a number of bits on the bus;

means for receiving from the bus a plurality of data words comprising multiword tokens;

means for receiving from the bus a complete address associated with the plurality of data words;

means for generating a series of addresses in RAM into which the buffered data words will be written;

means for writing the buffered data words into RAM at the generated addresses; and

means for buffering the received data words comprising:

at least three memory buffers for use as a swing buffer including an arrival buffer, an output buffer and at least one intermediate buffer;

a buffer manager for allocating said buffers for reference by said means for generating a series of addresses, clearing said buffers for occupation by subsequently arriving data, and maintaining status information of said buffers, wherein said status information comprises a state VACANT, wherein one of said buffers is available, a state IN... ... the bus an address and by said means for receiving from the bus a plurality of data words, a state FULL, wherein said one buffer is occupied by data, and a state READY; wherein said buffer manager asserts a late arrival signal indicating that a buffer in said state READY is not in synchronization with a data output rate... ... 1. An image formatter for processing encoded video data comprising:

an input element for receiving encoded data having a frame rate and an arrival rate;

a memory defining at least three buffers for storage of the encoded data, one of said buffers being a display buffer, and another of said buffers being an arrival buffer;

a write address generator for generating write addresses for data being stored thereat in said memory;

a read address generator for generating read addresses for reading data stored thereat in said memory;

an output interface linked to said read address generator that produces decoded data at a display rate; and

a buffer manager responsive to said arrival rate, said... ... 1. A pipeline machine, comprising a plurality of processing stages, characterized by:

two successive ones of said processing stages being connected by a two-wire link, wherein said two-wire link comprises:

a sender, a receiver, and a clock connected to said sender and said receiver, wherein data is transferred from said sender to said receiver upon a transition of said clock only when said sender is ready and said receiver is ready; wherein variable length tokens having data and control functions propagate across said two-wire link, said tokens each comprising a plurality of data words, each said word including an extension bit which indicates a presence or an absence of additional words in said token, a length of said token being determined by said extension bits; whereby said tokens are unlimited in length;

said processing stages comprising a spatial decoder accepting an encoded data stream having a plurality of video formats carried therein, said formats including at least an MPEG format;

a DRAM interface in said spatial decoder having a plurality of data buffers therein, and a RAM accepting data from said DRAM interface;

a coded data buffer;
a token generator, generating variable length tokens, a said variable length token comprising... ... END token and a FLUSH token;
means responsive to said PICTURE... ... END token for performing a stop-after-picture operation for achieving a clear end to picture data decoding, for indicating the end of a picture, and for clearing the pipeline; wherein responsive to said PICTUREEND token, data is cleared from said data buffers of said DRAM interface, and data in said coded data buffer is presented to a Huffman decoder of said spatial decoder, and responsive to said FLUSH token a portion of said processing stages are reconfigured to await arrival of further data... ... 1. A system for decoding video data and having a Huffman decoder, comprising:
an index to data (ITOD) stage, having a first mode of operation wherein an index number obtained from said Huffman decoder is converted into decoded data, and a second mode of operation wherein tokens received from said Huffman decoder are ignored, said tokens comprising a plurality
of data words, each said word including an extension indicator which indicates a presence or an absence of additional words in said token, a length of said token being determined by said extension indicators, whereby the length of said token can be unlimited;
an arithmetic logic unit (ALU); and
a data buffering means immediately following said system, whereby time spread for video pictures of varying data size can be controlled. 1. In a video decoding and decompression system having an input, an output and a plurality of processing stages between the input and the output defining a pipeline, the improvement comprising:
a token generator responsive to a data stream received via said input for generating an interactive interfacing control token, defining a universal adaptation unit, for data functions among said processing stages, wherein said token is variable in length and is... ... between a preceding member and a succeeding member of a pair of adjacent stages comprising an input data storage device (LDIN) and an output data storage device (LDOUT) in each member of said pair, with an output data storage device of the preceding member connected to an input data storage device of the succeeding member, the combination comprising:
validation circuitry in each said member to generate a validation signal (IN... ..... VALID) with a first state when data stored therein is valid and with a second state when data stored therein is invalid, said state defining the respective members ability to accept data;
said validation circuitry having at least one validation storage device (LVOUT) to store said validation signal of the respective member of said pair;
said pair of stages being connected by an acceptance line which conveys an acceptance signal (IN... ... ACCEPT, OUT

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